EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with John Guay on 7/9/2010.

a. Please enter the attached set of amended claims.

b. Please amend the title of the specification to read "Data processing architectures for packet handling wherein batches of data packets of unpredictable size are distributed across processing elements arranged in a SIMD array operable to process different respective packet protocols at once while executing a single common instruction stream".

REASONS FOR ALLOWANCE

2. The following is an examiner's statement of reasons for allowance.

The prior art of record does not teach or motivate that "the processing elements are arranged in a SIMD array and operable to process different respective packet protocols at once while executing a single common instruction stream" in the specific context of and in conjunction with the remaining limitations of the claim. While the

previously presented rejection of Marsan as modified by Clauberg teaches of distributing packets to a plurality of processing elements to be processed in an identical fashion, Marsan as modified by Clauberg does not disclose that the processing elements are arranged in a SIMD array and operable to process different respective packet protocols at once while executing a single common instruction stream. Examiner particularly notes that none of the pertinent prior art cited in pages 19-21 of the 1/21/2009 office action, nor the pertinent prior art cited below, would teach or render obvious the claimed limitations as a whole. Examiner further notes that none of the prior art cited by the previous examiner in this application would likewise teach or render obvious the claimed limitations as a whole.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

c. Nakayama et al. (US 6907001) discloses of a packet switch for switching variable length packets in the form of ATM cells.

d. John et al. (US 20030231627) discloses of arbitration logic for assigning input packet to an available thread of a multi-threaded multi-engine network processor.

e. Oskouy et al. (US 20020003795) discloses of in-line processing a data packet, wherein the step of storing the data packet in memory includes dividing the data packet into cells of a fixed size and storing the cells in a distributed memory.

f. Devanagondi et al. (US 7317730) disclose of load balancing for parallel packet processing in communication networks.

g. Donis et al. (US 20020075882) disclose of multiple priority buffering, wherein incoming cells have a fixed length, and the depth of a queue corresponds to the amount of information that can be stored in the particular queue.

h. Spencer (US 20050243829) discloses of distributing information about incoming packets amongst the PEs in an array.

i. Pham et al. (US 20030074388) disclose of distributing data packets to an array of packet processors, wherein the data packets are of different size.

j. Dyckerhoff et al. (US 7016367) disclose of allocating bandwidth for processing of packets, wherein a receive controller divides packets into a plurality of cells of a predetermined size.

k. Irwin (US 6393026) discloses of data packet processing being distributed to a processor array.

l. Laor et al. (US 6831923) disclose of a pipelined architecture wherein differing protocols use the same architecture.

m. Veal et al. (US 20100165991) discloses of SIMD processing of network packets.

n. Dorr et al. (US 20040017807) discloses of a plurality of processing elements, each operating according to a corresponding processing protocol.

o. Rai et al. (Packet Processing on a SIMD Stream Processor) disclose of a SIMD stream processing architecture for packet processing.

p. Seshadri et al. (A Case for Vector Network Processors) disclose of a SIMD approach to packet processing.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEITH VICARY whose telephone number is (571)270-1314. The examiner can normally be reached on Monday - Thursday, 7:00 a.m. - 5:30 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

/Keith Vicary/
Examiner, Art Unit 2183